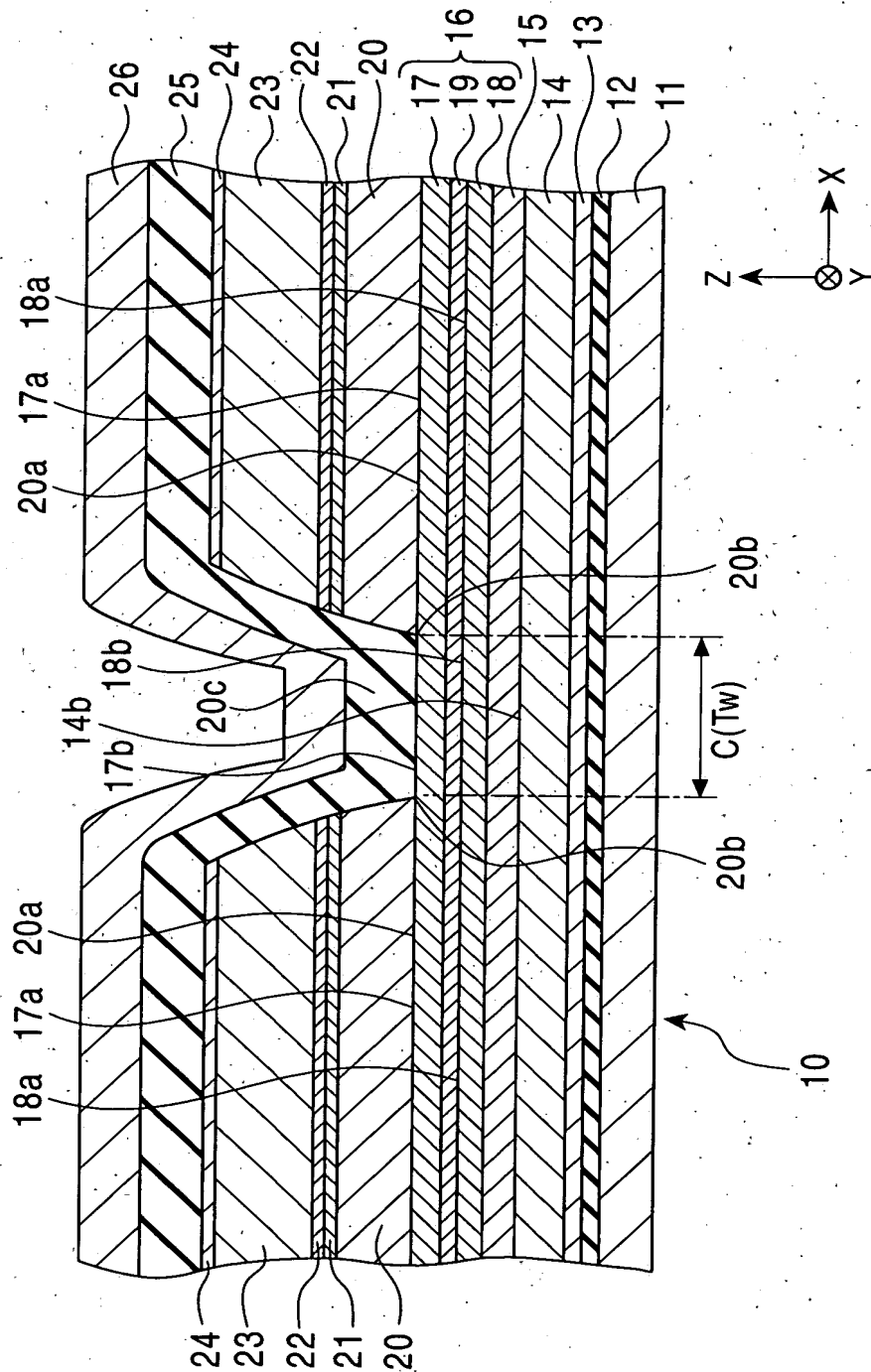
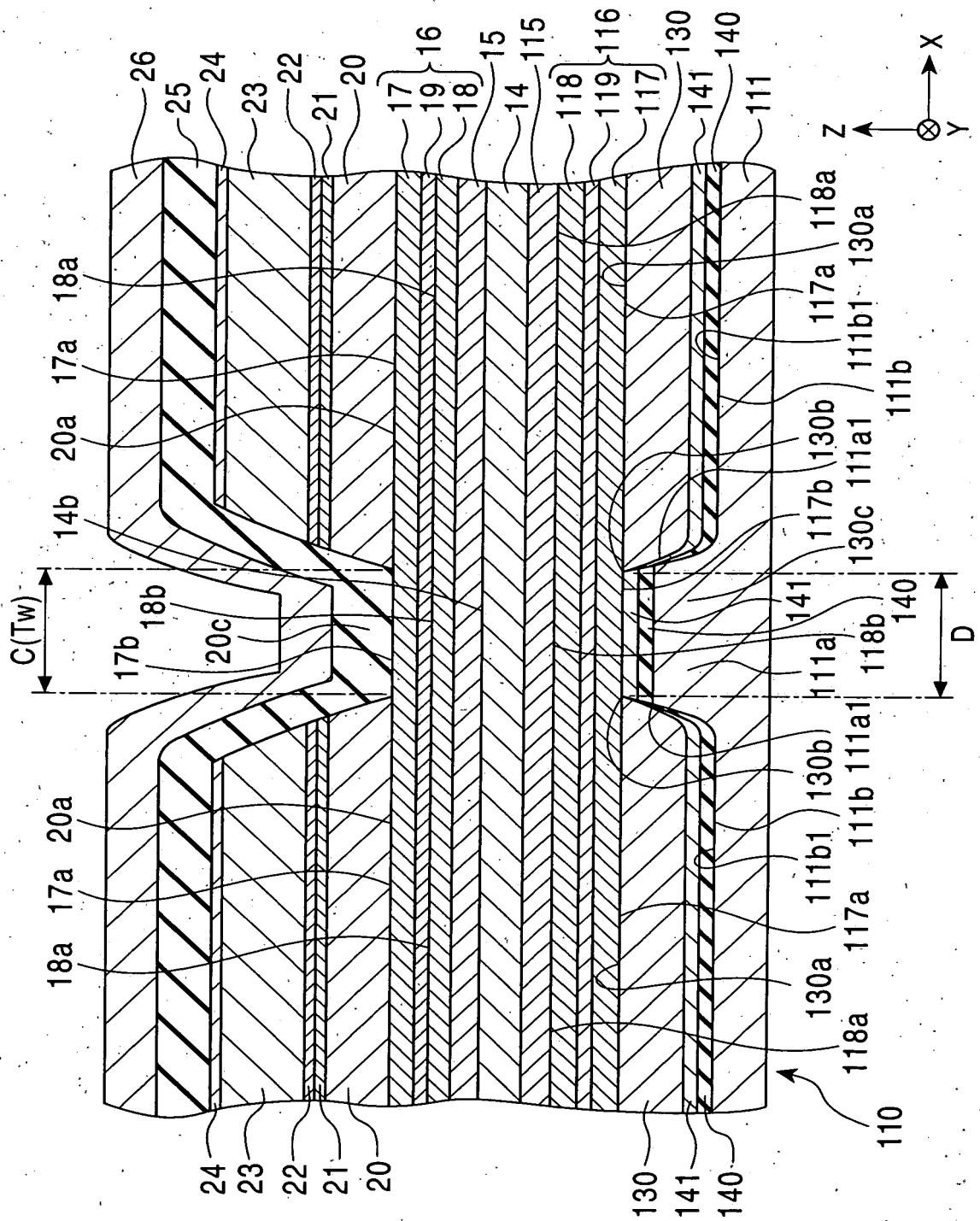


**FIG. 1**



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FIG. 2



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FIG. 3

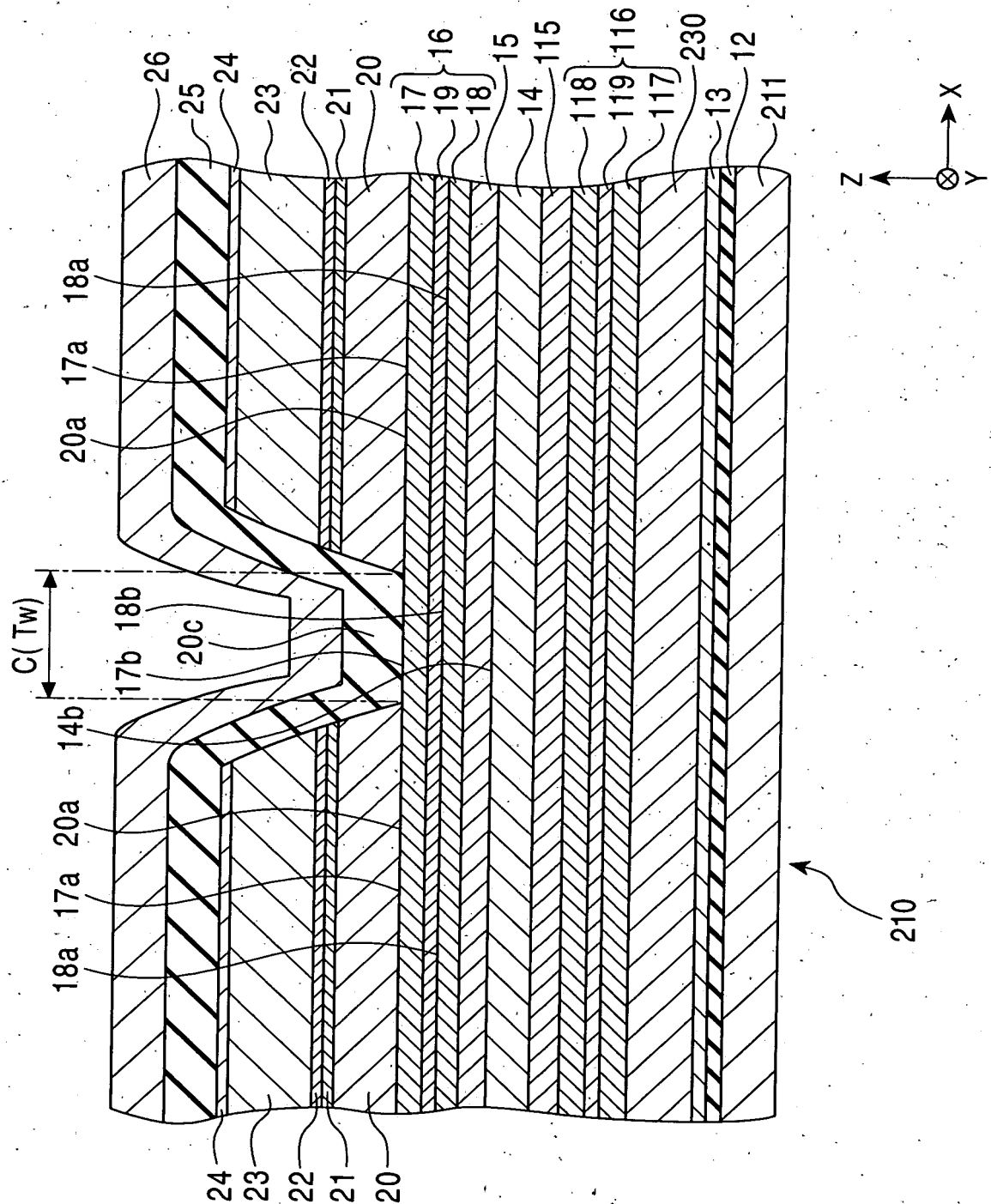


FIG. 4

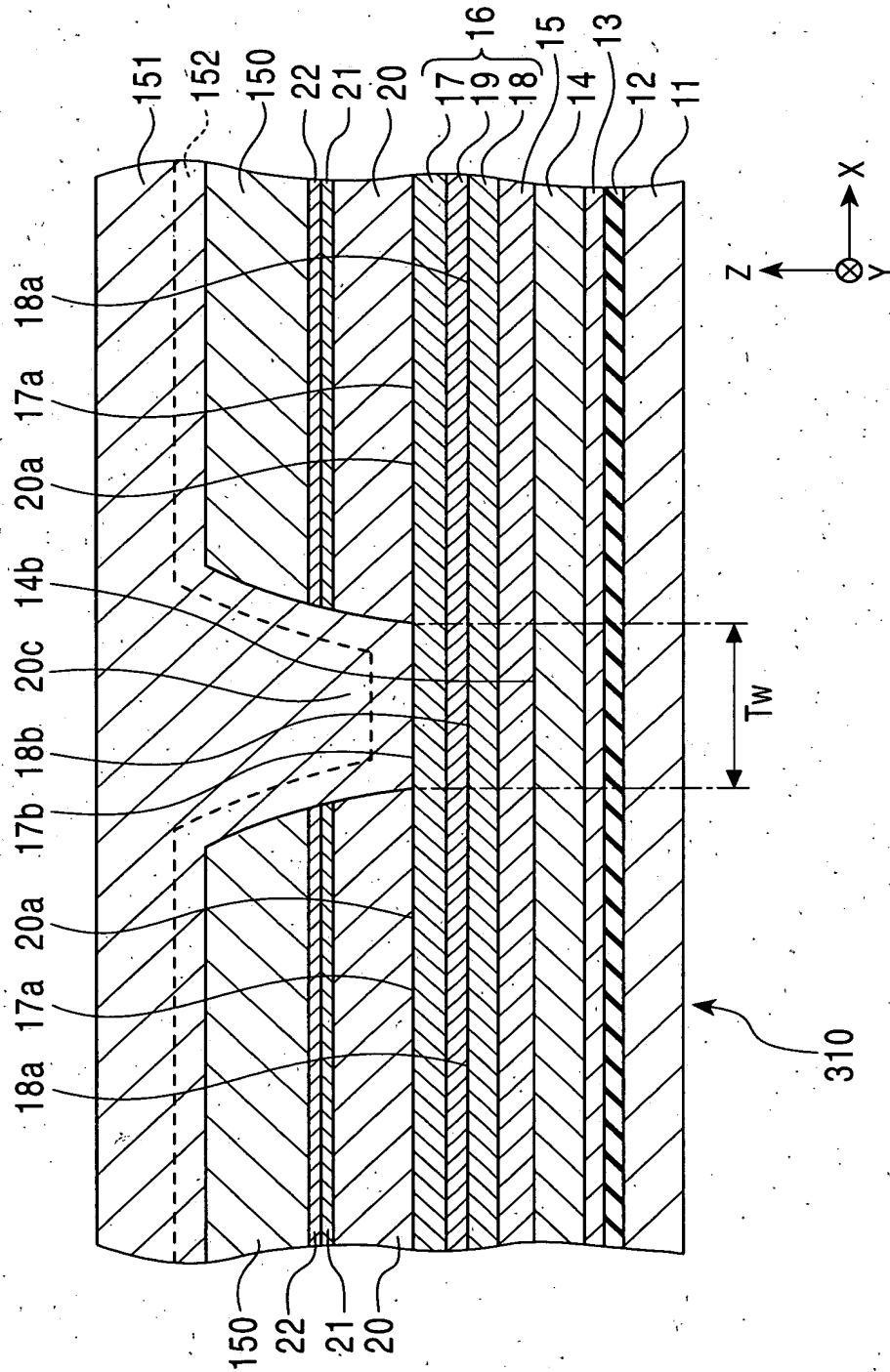
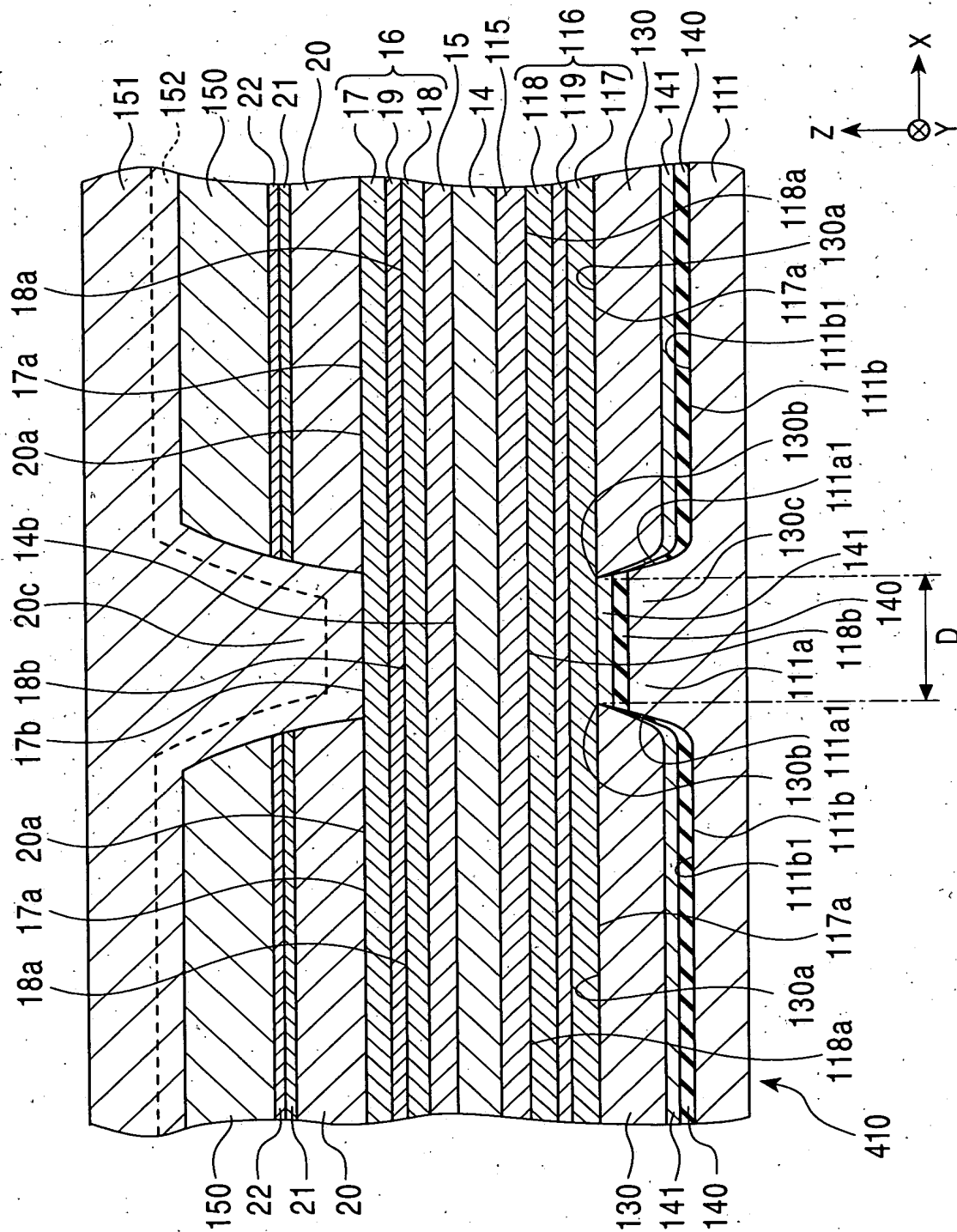
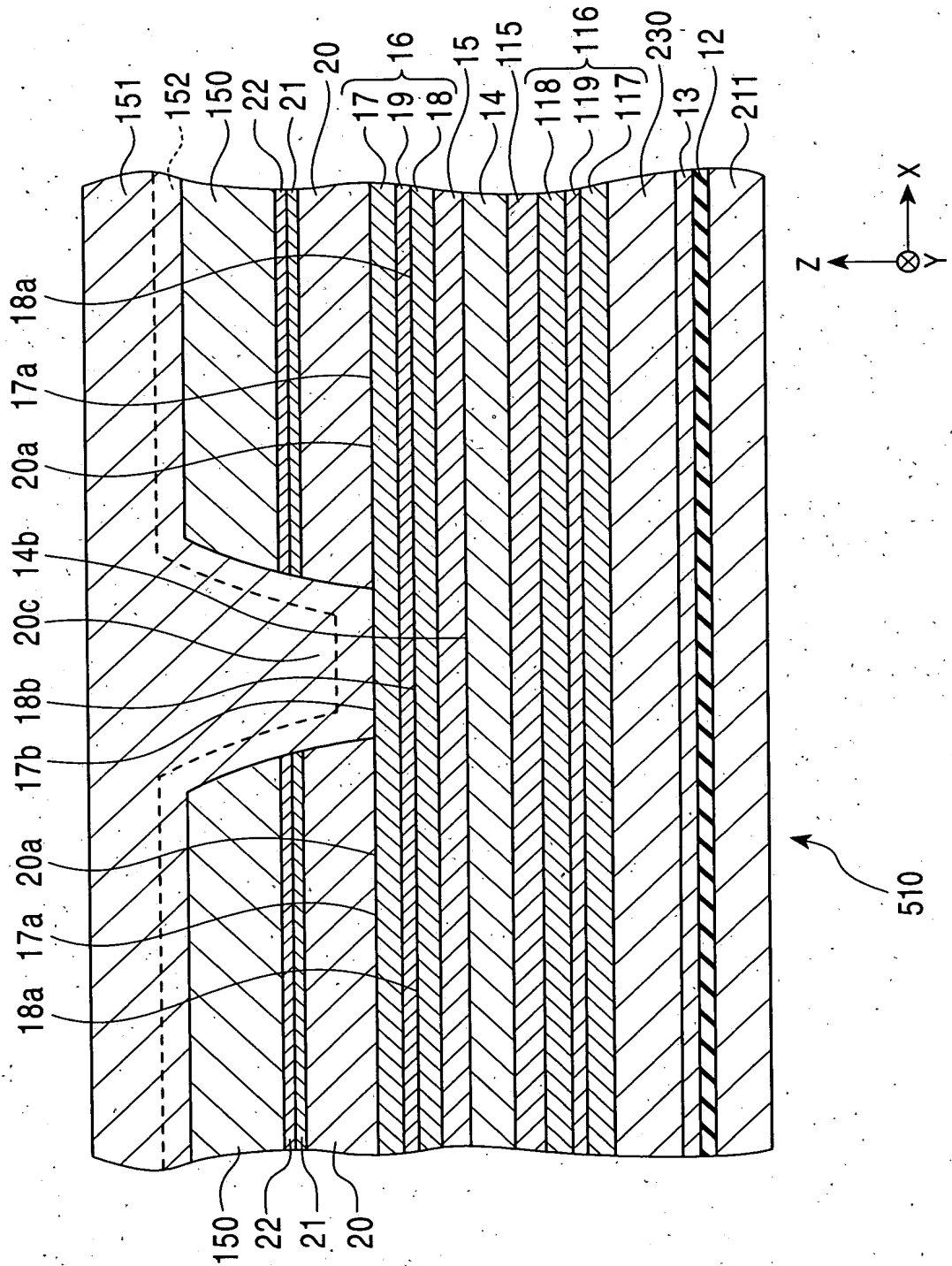


FIG. 5



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FIG. 6



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FIG. 7

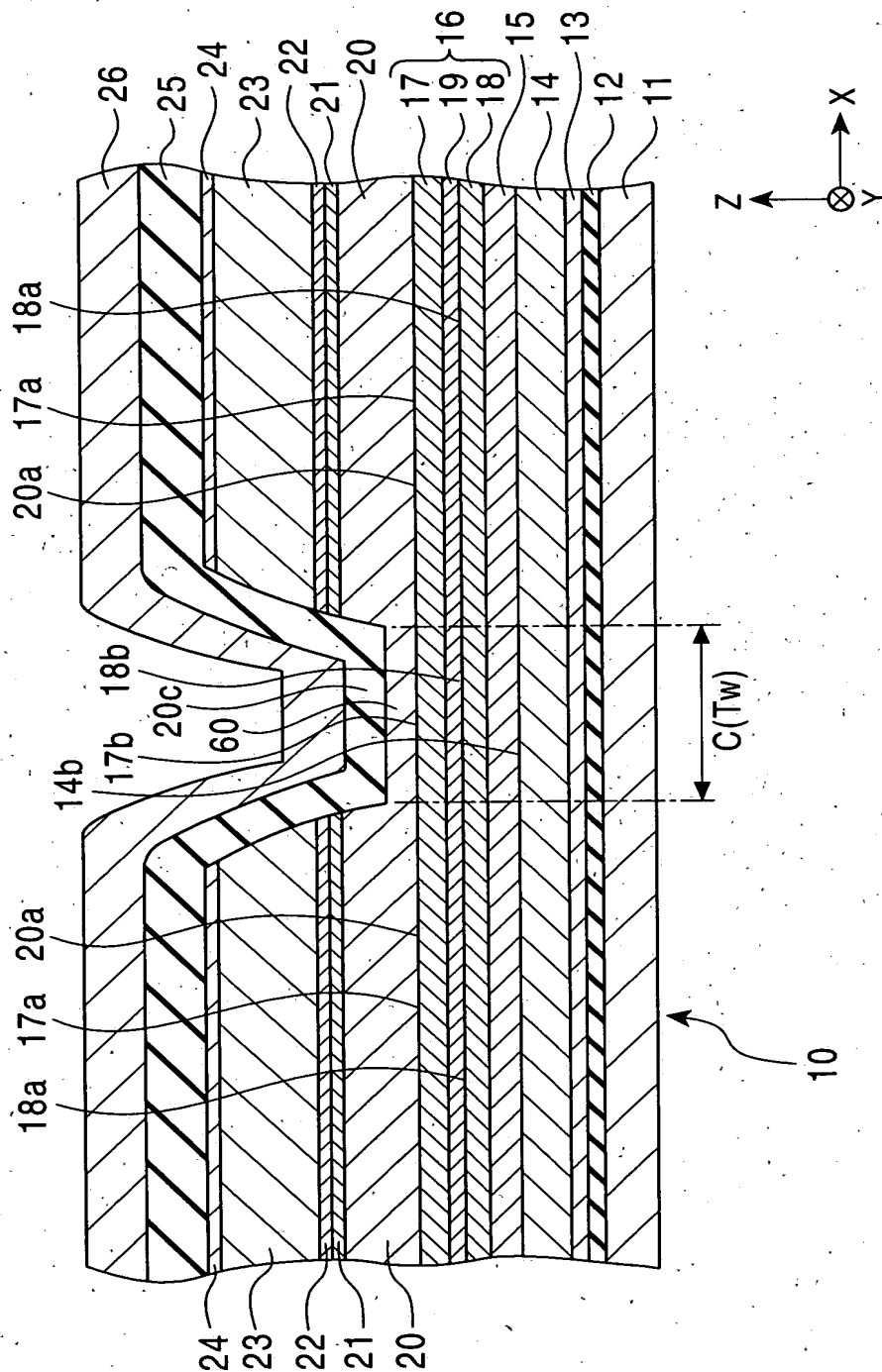


Figure 1 is a cross-sectional view of a semiconductor device 100. The device is shown in a cross-section along the Y-Z plane, with the X-axis pointing out of the page. The device consists of a substrate 110. On the left side, there is a gate stack 170 and a source/drain region 180. On the right side, there is a gate stack 130 and a source/drain region 140. The gate stacks are composed of a gate oxide 118, a gate dielectric 119, and a gate electrode 120. The source/drain regions are composed of a source/drain oxide 130, a source/drain dielectric 141, and a source/drain electrode 140. The channel 111 is defined by the gate oxide 118 and the source/drain oxide 130. The device is shown in a cross-section along the Y-Z plane, with the X-axis pointing out of the page. Dimensions C(Tw) and D are indicated.





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FIG. 10

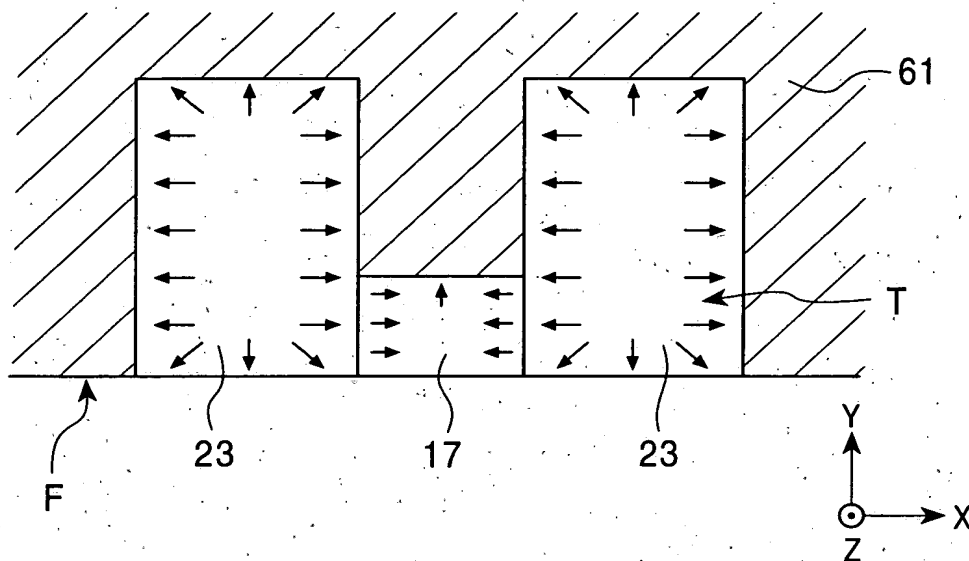
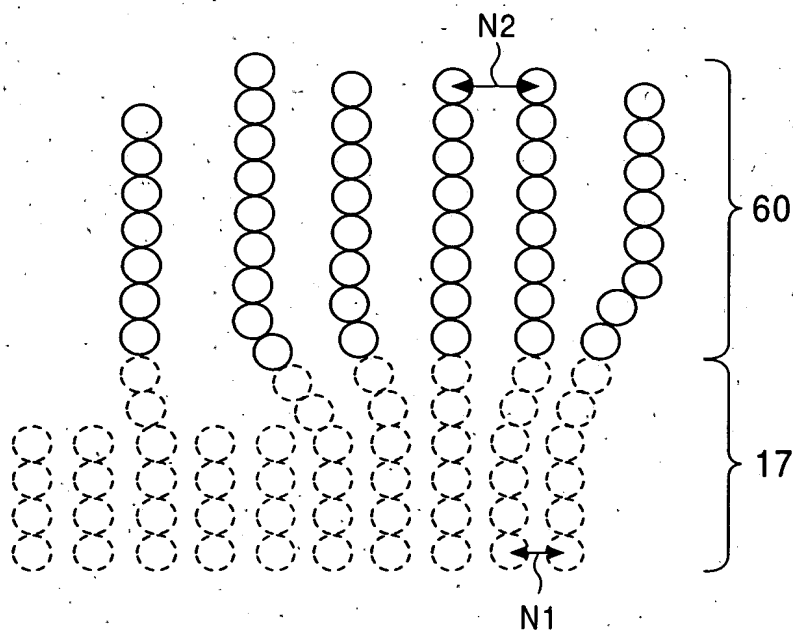


FIG. 11



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FIG. 12

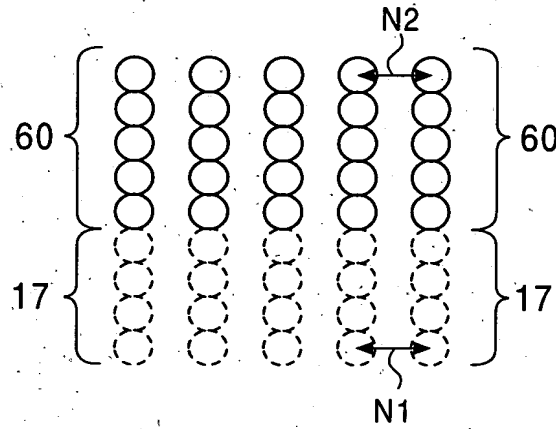
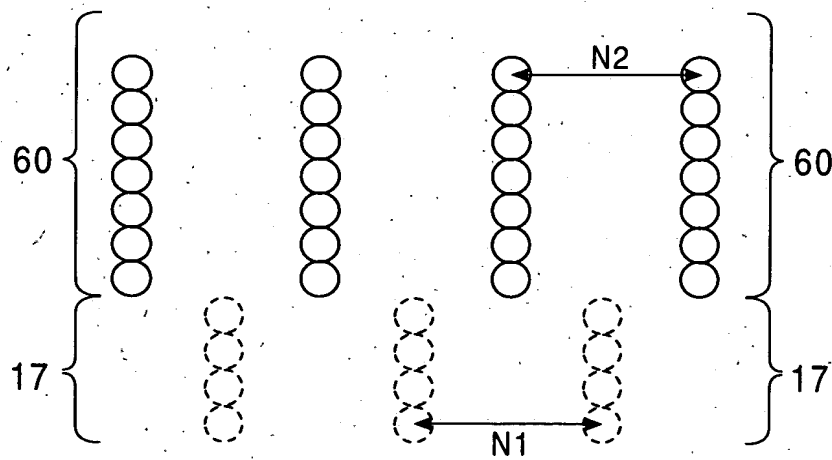


FIG. 13



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FIG. 14

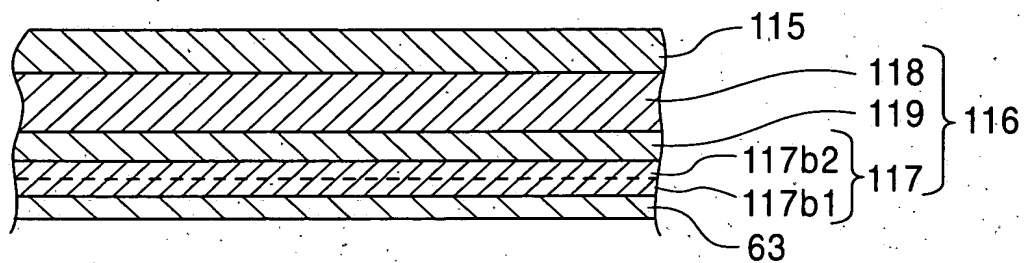


FIG. 15

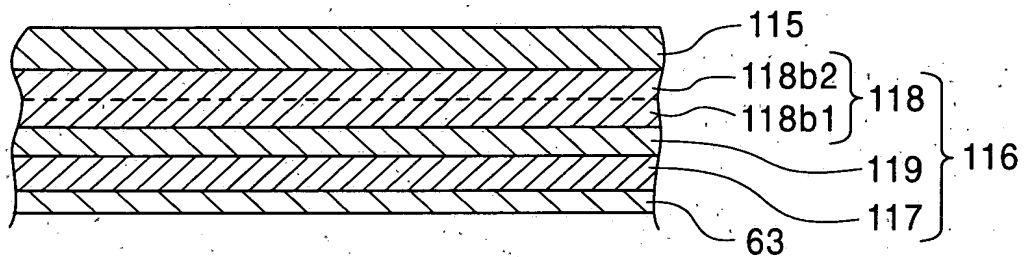
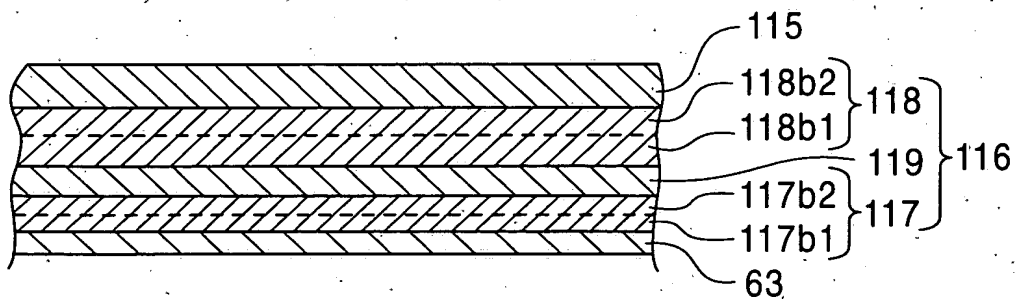
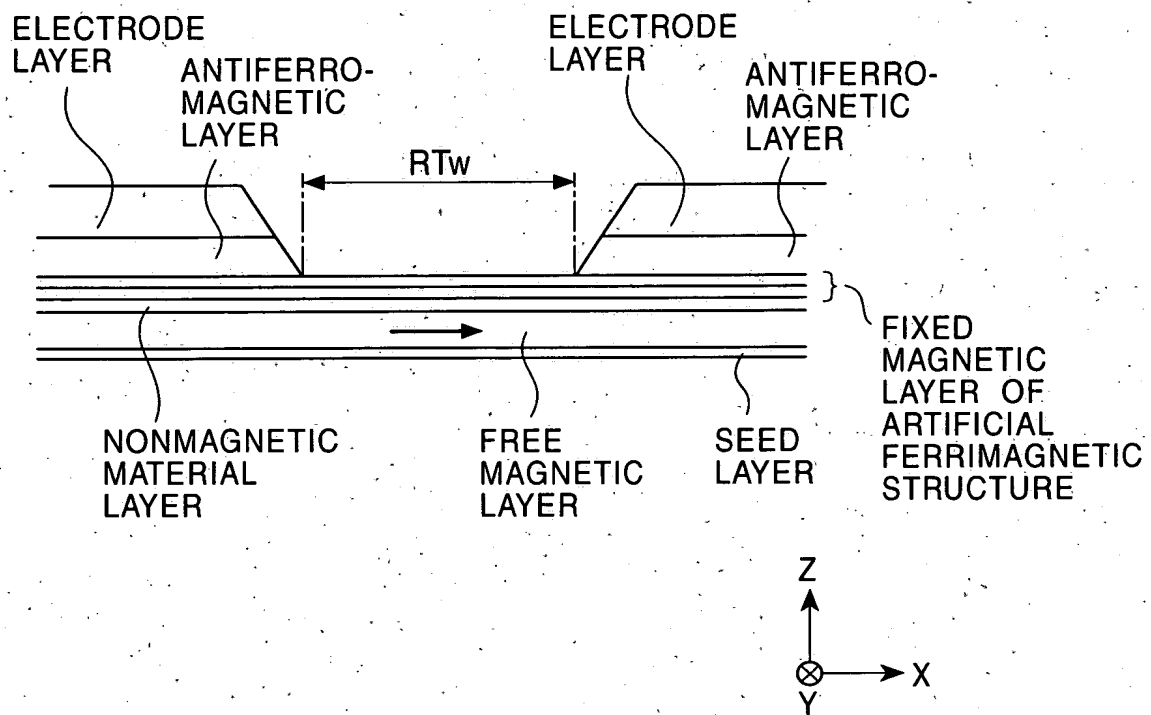


FIG. 16



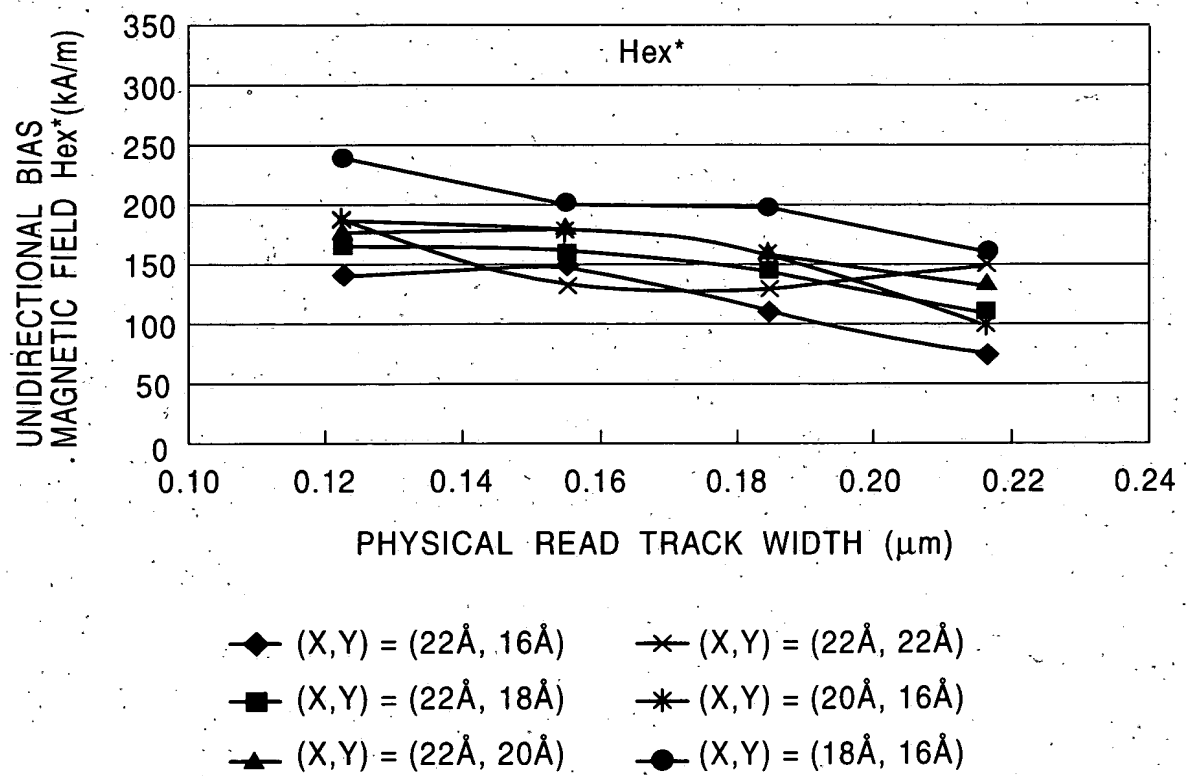
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FIG. 17



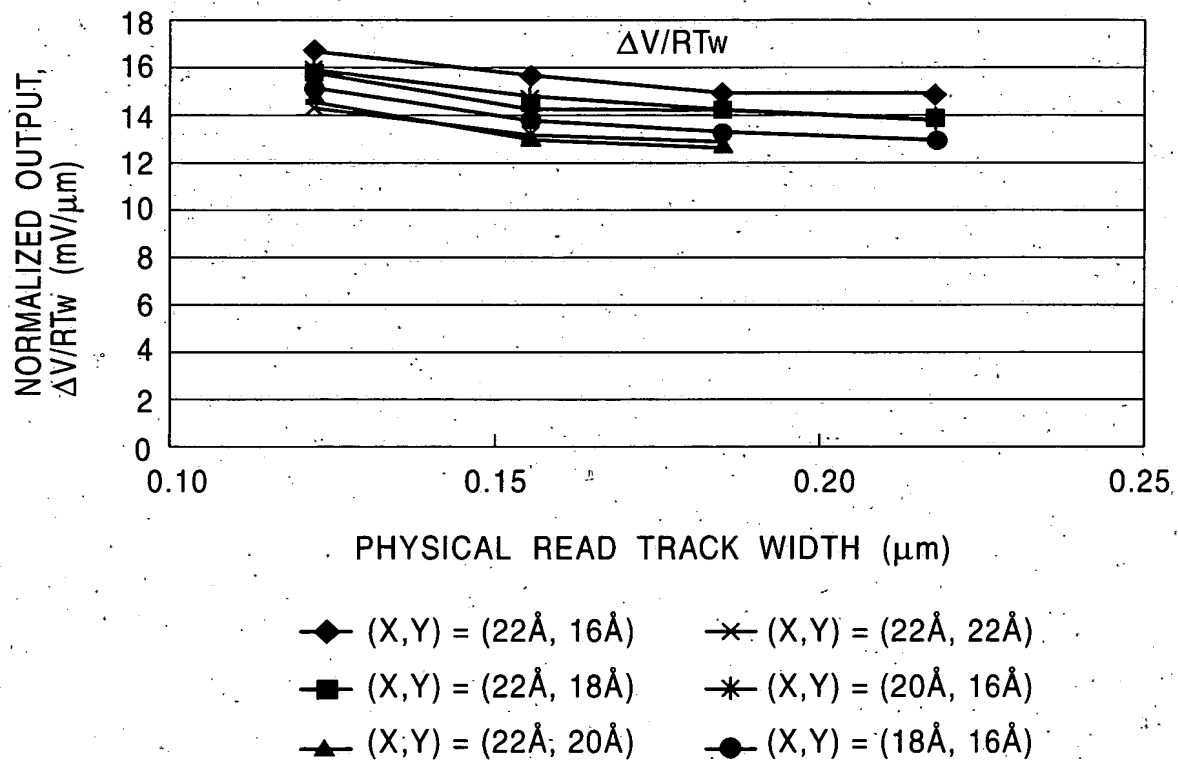
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FIG. 18



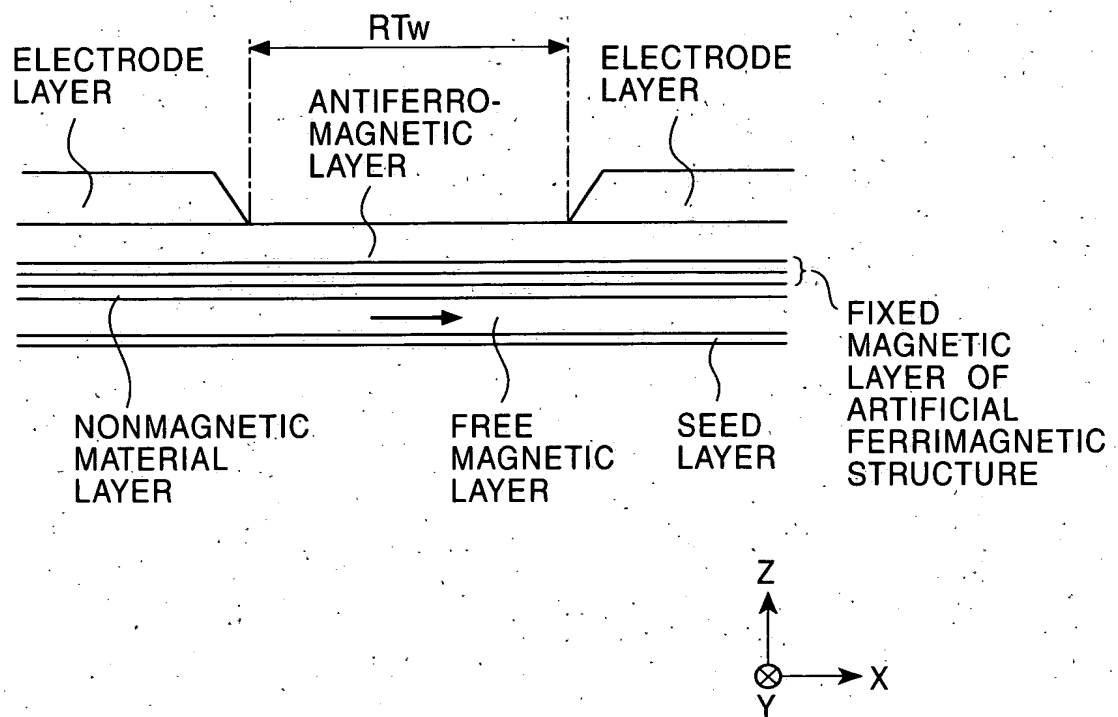
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FIG. 19



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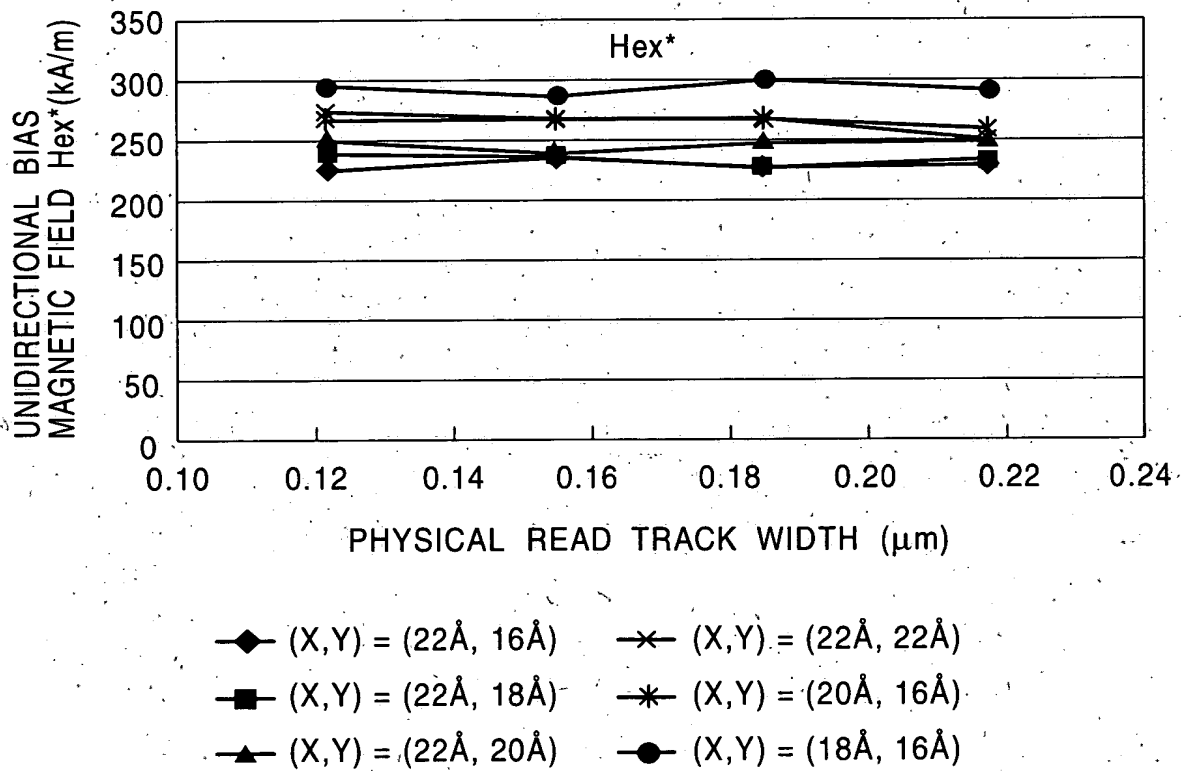
FIG. 20





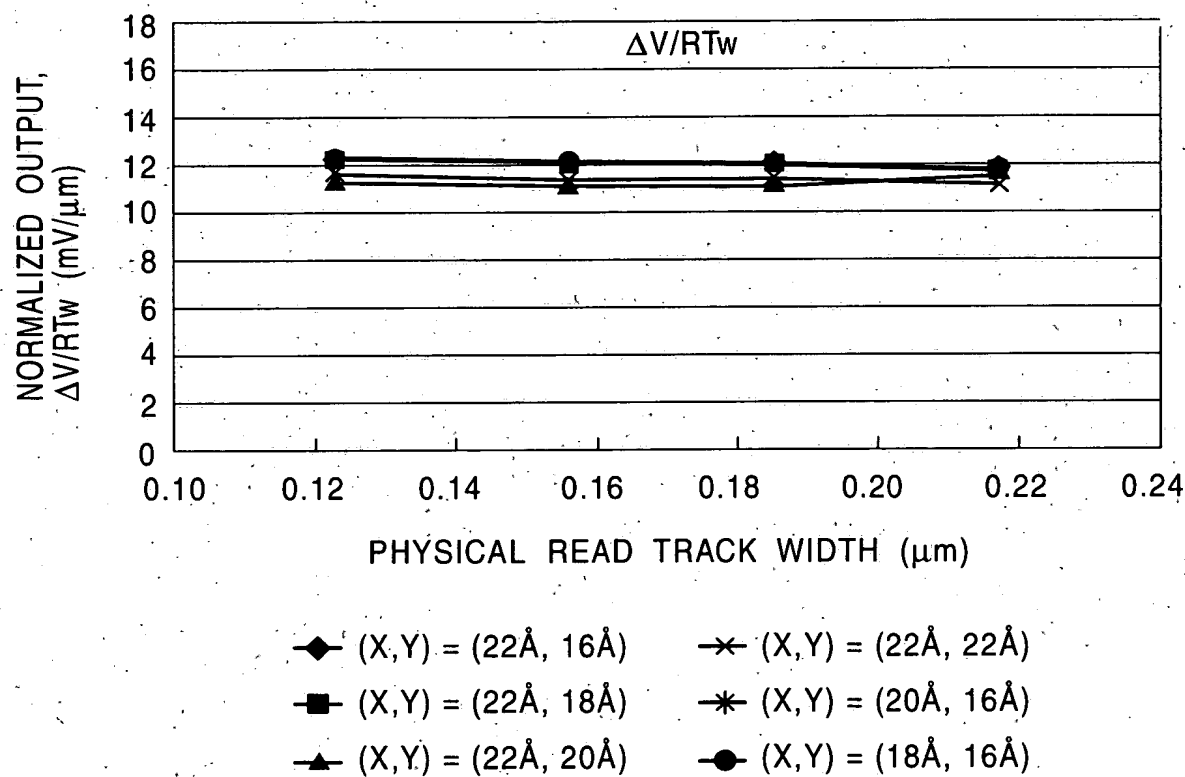
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FIG. 21



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FIG. 22



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FIG. 23

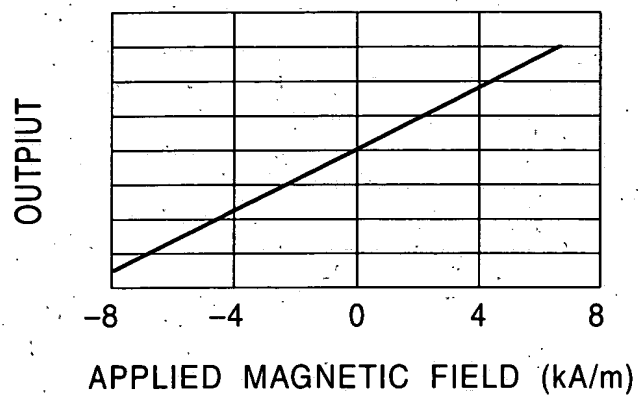
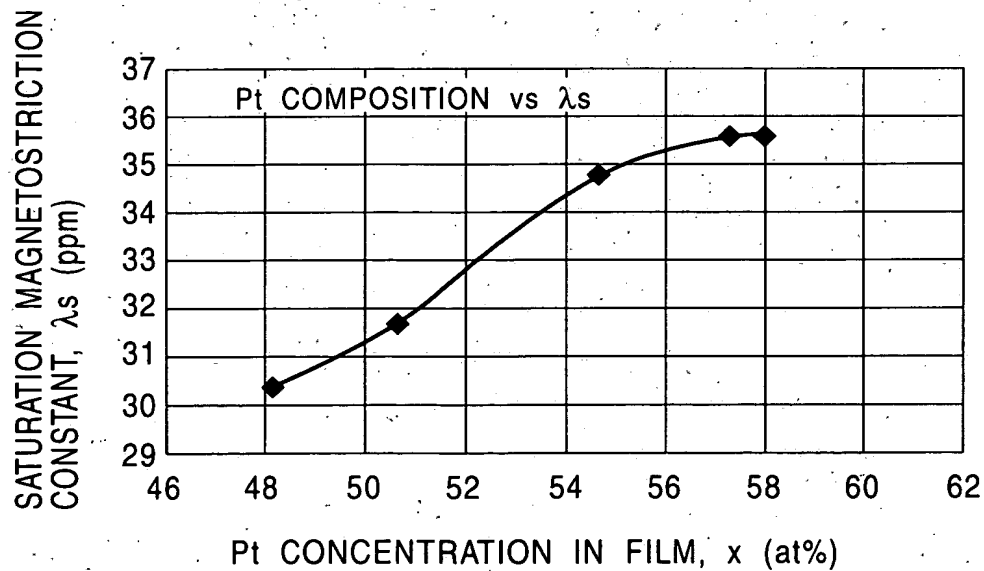


FIG. 24



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FIG. 25

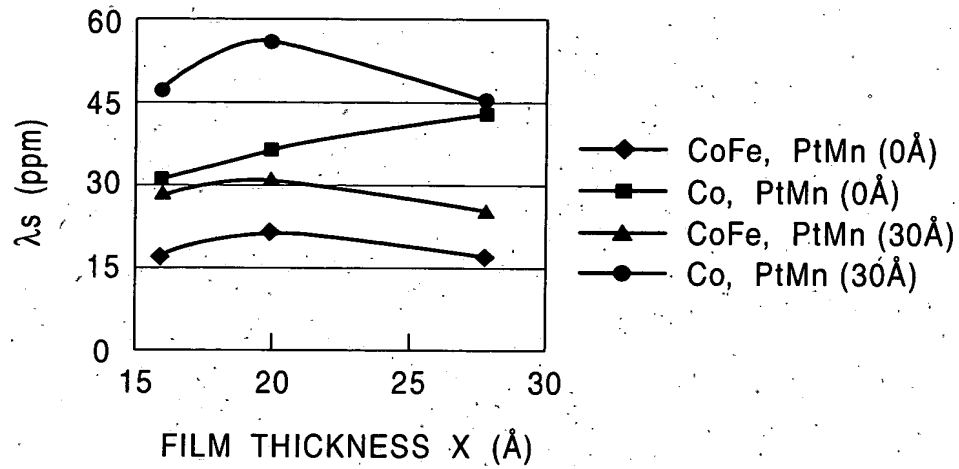


FIG. 26

